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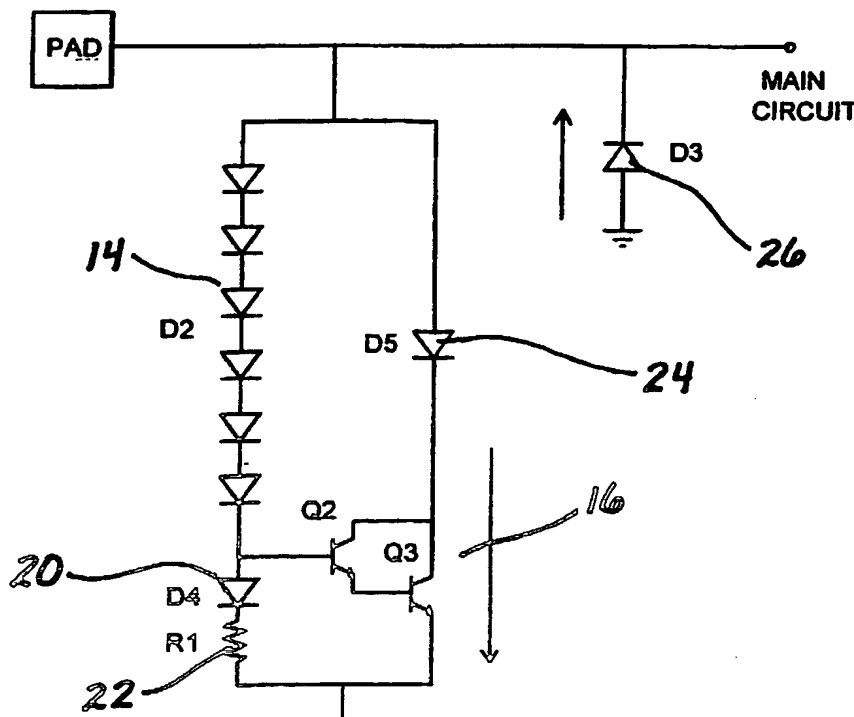
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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: ON-CHIP ESD PROTECTION CIRCUIT



(57) Abstract: A low loading capacitance on-chip electrostatic discharge (ESD) protection circuit for compound semiconductor power amplifiers is disclosed, which does not degrade the circuit RF performance. Its principle of operation and simulation results regarding capacitance loading, leakage current, degradation to RF performance are disclosed. The design, loading effect over frequency, robustness over process and temperature variation and application to an RF Power amplifier is presented in detail. The ESD circuit couples an input to ground during ESD surges through a diode string coupled to the input, and a transistor (28) switch or Darlington pair (16) having its gate coupled to and triggered by the diode string. The Darlington pair couples the input to ground when triggered through a low impedance path in parallel to the diode string (14). A reverse diode also couples ground to the input on reverse surges.

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INTERNATIONAL SEARCH REPORT

International application No.

PCT/US03/01420

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : H02H 9/00

US CL : 361/56

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 361/56, 111, 117-119

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
USPTO APS EAST

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2001/0017754 A1 (OKAWA) 30 August 2001 (30.08.2001) see figure 2A.	1,3,7,8,12,13,24-26, 29,30
Y,E	US 6,560,081 B1 (VASHCHENKO et al) 06 May 2003 (06.05.2003), see figure 2; column 2 lines 5-7.	1-30
Y,P	US 6,442,008 B1 (ANDERSON) 27 August 2002 (27.08.2002), see figure 1.	1-30
Y	US 5,528,189 A (KHATIBZADEH) 18 June 1996 (18.06.1996), see column 6, lines 1-6.	10

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

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27 May 2003 (27.05.2003)

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